

REMARKS

Claims 1-6 were objected to and rejected under §112, second paragraph. The claims are canceled without prejudice to reentry and the objection and rejection are moot.

The previous claims were rejected over Kimura JP '942, and that rejection is also moot. The new claims distinguish over Kimura as follows:

The first paragraph after the preamble in claim 7 recites that the conducting parts which are coupled to the integrated circuit of each chip are disposed on a front side of the chip. In the Applicant's Fig. 1, this front side faces up; in Kimura, the electrode 3 is on the downward face.

Kimura discloses (Figs. 2-4) providing a monolithic substrate 8 (Fig. 2(a)), and then forming an insulator 6b on the downward face (Fig. 2(d)). Only later, in step 3(h), are holes are formed in the substrate 8. Then, in step 3(i), the holes are filled with a different insulator 6(c). Finally, the chips are separated, in Fig. 4(n).

Claim 7 distinguishes over Kimura by reciting that chips are prepared, then arranged, and then the spaces between are filled with an insulating material on the front side of each chip. Kimura does not prepare and then arrange chips; the chips are separated only at the very end, and there is no disclosure of "arranging" or "disposing" anything.

Furthermore, Kimura uses two steps and two different insulating materials where the Applicant uses one, in "filling an insulating material on the front side of each of the semiconductor chips and in the clearance between the semiconductor chips " (claim 7). Claim 7 distinguishes, and new claim 13 further distinguishes, over Kimura's two distinct insulating steps of Figs. 2(d) and 4(l).

New claims 15-16 are not disclosed or suggested by Kimura, because the conductive layer 5b is covered over with insulation 6d.

Horiuchi Publication '010 also fails to disclose the claimed subject matter.

Allowance is requested.

Respectfully submitted,



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